What is claimed is:

1. An equalizer circuit comprising:

carrier sensing means for sensing the start of a reception signal on the basis of a signal representing a reception level of the reception signal;

first and second equalizing means for equalizing the reception signal;

control means for alternately enabling said first and second equalizing means every frame reception in accordance with an output from said carrier sensing means; and

switching means for alternately switching between outputs from said first and second equalizing means every frame reception and outputting the selected output as demodulation data.

2. A circuit according to claim 1, wherein

said control means alternately outputs first and second carrier sense signals to said first and second equalizing means for a time interval from time when the detection signal is output from said carrier sensing means to time when equalizing processing is complete in said first and second equalizing means, and

said first and second equalizing means alternately equalize the reception signal every frame reception in response to first and second carrier sense

signals from said control means.

3. A circuit according to claim 2, further comprising first and second gate means for receiving a system clock signal and the first and second carrier sense signals from said control means and supplying an output clock signal to said first and second equalizing means.

4. A circuit according to claim 2, wherein

said first and second equalizing means output first and second demodulation data used during equalizing processing to said switching means and output first and second demodulation data gate signals synchronized with the first and second demodulation data to said control means and said switching means,

said control means stops outputting the first and second carrier sense signals in response to the first and second demodulation data gate signals, and

said switching means alternately outputs the first and second demodulation data in response to the first and second demodulation data gate signals.

5. A circuit according to claim 2, wherein

said first and second equalizing means comprise equalizers for setting tap coefficients and memories for storing preamble signals of the reception

signal, and

said first and second equalizing means detect frequency offset values, estimate transmission line characteristics, and set the tap coefficients at the start of reception of the reception signal.

6. An equalizing method comprising the steps of:

detecting the start of a reception signal on the basis of a signal representing a reception level of the reception signal;

alternately enabling first and second equalizer units for equalizing the reception signal upon detecting the start of the reception signal; and

alternately switching between outputs from said first and second equalizer units every frame reception and outputting the selected output as demodulation data.

7. A circuit according to claim 4, wherein the step of alternately enabling further comprises the step of alternately outputting first and second carrier sense signals as enable signals to said first and second equalizer units for a time interval from time when the start of the reception signal is detected to time when equalizing processing is complete in said first and second equalizer units.

8. A circuit according to claim 5, further comprising the step of alternately supplying a system clock signal to said first and second equalizer units in accordance with the first and second carrier sense signals.

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